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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/979,572	BHARDWAJ ET AL.	
	Examiner	Art Unit	
	Aimee J. Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43,75 and 76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *75 and 76* is/are allowed.

6)☒ Claim(s) *1-24 and 26-43* is/are rejected.

7)☒ Claim(s) *25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-43 and new claims 75-76 have been considered. New claims 75-76 have been added as per Applicant's request. Claims 44-74 have been cancelled as per Applicant's request. Claims 1, 6, 8, 11, 16, 18-20, 22, 24, 26, 31-33, and 39 have been amended as per Applicant's request.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment as filed 25 October 2005; Extension of Time for One Month as received on 25 October 2005; and Amendment as received on 26 January 2006.

Allowable Subject Matter

3. Claim 25 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

4. Claims 75-76 are allowed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-24 and 26-43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farber et al., U.S. Patent Number 4,516,203 (herein referred to as Farber) in view of Allen et al., "A Program Data Flow Analysis Procedure" ©1976 (herein referred to as Allen).

7. Referring to claim 1, Farber has taught a processor comprising:

a. Instructions with at least one operand field, the instructions comprises immediate instructions having immediate data in the operand field (Farber column 14, lines 39 to column 15, line 9; column 24, lines 10-20; Figure 2; and Figure 7);

b. A data table for storing immediate data of immediate instructions, wherein the data table enables immediate data to be separated from the instruction stream (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2). In regards to Farber, a data table, in the broadest reasonable interpretation, is a collection of data (See FOLDOC's "table"). Farber's cache contains encacheable data, e.g. a collection of data, which are directly accessed and not changed throughout execution of the procedures, e.g. immediate constants, without having the immediate constants specified within the instruction, e.g. separated from the instruction stream.

c. A program counter for storing an instruction address of an instruction, wherein the processor fetches an instruction from the instruction address in the program counter during program execution (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8); and

d. An instruction decoder for decoding the instruction fetched by the processor (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

e. Wherein immediate data from the data table is provided to the processor if the instruction fetched is an immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

8. Farber has not taught wherein immediate data are stored in the data table in an order determined by a flow analysis. However, Farber has taught that the immediate data is stored in a data table (See rejection above). Allen has taught data flow analysis shows what data is "live" during the flow of a program and where the program would profit from having the data stored (Allen Abstract; page 137, column 2, paragraph 2; page 138, column 1, paragraph 2; page 146, column 1, paragraph 5). A person of ordinary skill in the art at the time the invention was made would have recognized data flow analysis allows instructions to be executed as soon as their inputs are available (See FOLDOC's "data flow analysis"), thereby increasing processor speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the data flow analysis of Allen in the device of Farber to increase processor speed.

9. Referring to claims 2 and 10, Farber in view of Allen has taught

a. An instruction register coupled to the instruction decoder (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8);

b. The instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to

column 29, line 33; and Figure 8). In regards to Farber, the I-stream Reader inherently has an instruction register in order to generate the outputs necessary.

10. Referring to claim 3, Farber in view of Allen has taught wherein the instruction register is coupled to the data table (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the instruction register provides an address of the immediate data in the data table when the immediate instruction is decoded by the instruction decoder (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

11. Referring to claims 4, 8, and 13, Farber in view of Allen has taught a data table addressing unit coupled to the instruction decoder and the data table (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the data addressing unit providing an address of the immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

12. Referring to claims 5 and 9, Farber in view of Allen has taught wherein the data table addressing unit comprises a data table pointer for storing the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

13. Referring to claims 6 and 11, Farber in view of Allen has taught

a. Wherein the instruction register is coupled to the data table addressing unit (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

b. The instruction register passes addressing information to the data table addressing unit to provide the address when the immediate instruction is decoded by the instruction decoder (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

14. Referring to claims 7 and 12, Farber in view of Allen has taught wherein the data table addressing unit comprises a data table pointer for storing the addressing information which serves as the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

15. Referring to claim 14, Farber in view of Allen has taught wherein the data table addressing unit comprises an incrementor, the incrementor increments the address after the immediate data is provided to produce a new address for a new immediate instruction (Farber column 28, lines 37-38). In regards to Farber, in order to increment the PC register, there must inherently be an incrementor to produce a new address.

16. Referring to claim 15, Farber in view of Allen has taught wherein the data table addressing unit comprises:

a. A data table pointer for storing the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. An incrementor, the incrementor increments the address in the data table pointer after the immediate data is provided to produce a new address in the data table pointer for a next immediate instruction executed by the processor (Farber column 28, lines 37-38). In regards to Farber, in order to increment the PC register, there must inherently be an incrementor to produce a new address.

17. Referring to claim 16, Farber in view of Allen has taught wherein the incrementor comprises an adder, the adder is coupled to the data table pointer, the adder adds the address in the table pointer and an index to produce the new address (Farber column 28, lines 37-38). In regards to Farber, in order to increment the PC register, there must inherently be an adder to produce a new address.

18. Referring to claim 17, Farber in view of Allen has taught wherein the index comprises a 1 (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

19. Referring to claim 18, Farber in view of Allen has taught wherein an addressing information is passed to the data table addressing unit, the addressing information comprises an index for indexing the address to produce a new address of another immediate data in the data

table for another immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

20. Referring to claim 19, Farber in view of Allen has taught wherein addressing information is passed to the data table addressing unit, the addressing information comprises an index for indexing the address to produce a new address pointing to a next immediate data in the data table for a next immediate instruction fetched by the processor (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

21. Referring to claim 20, Farber in view of Allen has taught

a. An instruction register coupled to the instruction decoder and the data table addressing unit (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

b. The instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for decoding (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8),

c. When the decoder decodes the immediate instruction, the instruction register passes the addressing information contained in the instruction to the data table addressing unit (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to

column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

22. Referring to claim 21, Farber in view of Allen has taught wherein the data table addressing unit comprises:

a. A data table pointer for storing the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. An adder for adding the addressing information to the address after the immediate data is provided to produce a new address in the data table pointer for a next immediate instruction executed by the processor (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

23. Referring to claim 22, Farber in view of Allen has taught

a. An instruction register coupled to the instruction decoder (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the instruction register stores the instruction fetched by the processor during program execution and passes the instruction to the instruction decoder for

decoding (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8); and

b. A data table addressing unit coupled to the data table and the instruction register (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8), the instruction register passing relative addressing information contained in the instruction to the data table addressing unit when the decoder decodes the immediate instruction, the relative addressing information, which comprises an index and a format indicator, is used to provide an address of the immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

24. Referring to claim 23, Farber in view of Allen has taught wherein the data addressing unit comprises a data table pointer containing a value,

a. If the format indicator comprises a post-format, the value serves as the address and after the immediate data is provided to the processor, the index is added to the value to produce a new value in the data table pointer for a next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2), and

b. If the format indicator comprises a pre-format, the index is added to the value to produce the address to the immediate data and the address is incremented by 1 after the immediate data is provided to the processor to produce a new value in the data table pointer for the next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

25. Referring to claim 24, Farber in view of Allen has taught wherein the format indicator comprises a binary bit having a logic 1 and logic 0 value, the logic 1 indicating the pre-format and the logic 0 indicating the post-format (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

26. Referring to claim 26, Farber in view of Allen has taught wherein the flow analysis comprises a static flow analysis, the static flow analysis identifies immediate instructions within a program (Allen Abstract; page 137, column 2, paragraph 2; page 138, column 1, paragraph 2; page 146, column 1, paragraph 5).

27. Referring to claim 27, Farber in view of Allen has taught wherein an immediate instruction comprises addressing information to enable the processor to retrieve a corresponding immediate data to the immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-

42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

28. Referring to claim 28, Farber in view of Allen has taught wherein the addressing information comprises absolute addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

29. Referring to claim 29, Farber in view of Allen has taught wherein the addressing information comprises relative addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

30. Referring to claim 30, Farber in view of Allen has taught data addressing unit coupled to the data table, the data addressing unit receives the relative addressing information and produces an address to the corresponding immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

31. Referring to claim 31, Farber has taught a method of executing instructions in a processor by separating immediate data of immediate instructions from an instruction stream comprising:

a. Identifying immediate data from the program (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9,

lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2) and

b. Storing the immediate data in a data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

32. Farber has not taught performing a flow analysis on a program having instructions which includes immediate instructions having immediate data, and storing the immediate data in an order determined by the flow analysis. However, Farber has taught that the immediate data is stored in a data table (See rejection above). Allen has taught data flow analysis shows what data is "live" during the flow of a program and where the program would profit from having the data stored (Allen Abstract; page 137, column 2, paragraph 2; page 138, column 1, paragraph 2; page 146, column 1, paragraph 5). A person of ordinary skill in the art at the time the invention was made would have recognized data flow analysis allows instructions to be executed as soon as their inputs are available (See FOLDOC's "data flow analysis"), thereby increasing processor speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the data flow analysis of Allen in the device of Farber to increase processor speed.

33. Referring to claim 32, Farber in view of Allen has taught wherein separating the immediate data from the instruction stream comprises:

a. Fetching an instruction from a program (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8);

b. Decoding the instruction to determine a type of instruction (Farber column 27, line 42 to column 28, line 15; column 28, line 63 to column 29, line 33; and Figure 8); and

c. If the instruction comprises an immediate instruction, fetching an immediate data corresponding to the immediate instruction from a data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

34. Referring to claim 33, Farber in view of Allen has taught wherein the immediate data of the immediate instructions are stored in the data table in an order determined by the flow analysis for identifying the immediate instructions in a program (Allen Abstract; page 137, column 2, paragraph 2; page 138, column 1, paragraph 2; page 146, column 1, paragraph 5).

35. Referring to claim 34, Farber in view of Allen has taught providing addressing information for fetching the immediate data from the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

36. Referring to claim 35, Farber in view of Allen has taught wherein the immediate instruction provides the addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10,

lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

37. Referring to claim 36, Farber in view of Allen has taught storing the addressing information in a data table pointer (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

38. Referring to claim 37, Farber in view of Allen has taught wherein the addressing information comprises relative addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

39. Referring to claim 38, Farber in view of Allen has taught processing the relative addressing information by a data table addressing unit to generate an address for fetching the immediate data from the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

40. Referring to claim 39, Farber in view of Allen has taught wherein processing the relative addressing information comprises:

a. Using a value stored in a data pointer of the data addressing unit to serve as the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column

2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. After fetching the immediate data, adding the relative addressing information to the value to produce a next address in the data table for fetching a next immediate data for a next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

41. Referring to claim 40, Farber in view of Allen has taught wherein the addressing information comprises an index and a format indicator (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

42. Referring to claim 41, Farber in view of Allen has taught wherein processing the relative addressing information comprises:

a. If the format indicate comprises a post-format,

i. Using a value stored in a data pointer of the data addressing unit to serve as the address (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2), and

ii. After fetching the immediate data, adding the index to the address to produce a next address in the data table for fetching a next immediate data for a next immediate instruction (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. If the format indicator comprises a pre-format,

i. Adding the index to the value to serve as the address for fetching the immediate data in the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2), and

ii. Incrementing the address after the immediate data is fetched to produce a next address in the data table for fetching a next immediate data for a next immediate instruction (Farber column 28, lines 37-38).

43. Referring to claim 42, Farber in view of Allen has taught wherein the addressing information comprises relative addressing information (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2).

44. Referring to claim 43, Farber in view of Allen has taught wherein providing the relative addressing information comprises:

a. Using a value in a data pointer to provide the addressing information to fetch the immediate data from the data table (Farber column 1, lines 26-29, 35-40, 53-58; column 1, line 62 to column 2, line 6; column 5, lines 8-24; column 9, lines 16-31; column 10, lines 39-42; column 12, line 31 to column 13, line 6; column 14, line 39 to column 15, line 9; column 15, lines 28-64 and Figure 2); and

b. Incrementing the value to provide a new addressing information for fetching another immediate data for a subsequent immediate instruction fetched by the processor (Farber column 28, lines 37-38).

Response to Arguments

45. Applicant's arguments with respect to claims 1-24 and 26-43 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

46. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Goddard et al., U.S. Patent Number 5,761,105, has taught a table storing constant values in order to separate them from the instructions.

b. Lloyd D. Fosdick and Leon J. Osterweil "Data Flow Analysis in Software Reliability" © 1979 has taught performing data flow analysis.

c. FOLDOC's "record" and "static analysis" provide further explanation and clarification for terms.

47. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

48. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J. Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:00am-4:30pm.

50. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

51. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
31 March 2006

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100